ABSTRACT

A scheme for freezing the clock of a CSOC to obtain a static view of the hardware for debugging purposes. A breakpoint unit is programmed to break on specific conditions or sequence of events. The breakpoint unit monitors the bus. Upon the occurrence of the programmed event the breakpoint unit generates a clock freeze signal. The clock freeze event signal is input to the bus arbiter which causes the bus arbiter to stop granting access to the bus to any bus master except the debug port. The bus arbiter checks for pending transactions on the bus and monitors the completion of any pending transactions. This ensures that the system will not be frozen while in a wait state which would render the bus inoperable. Once all pending transactions are complete, the bus arbiter generates a qualified clock freeze signal to the CSL clock thereby freezing the system for debugging.